DDR Termination Regulator

DESCRIPTION

The EUP7997 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7997 contains a high-speed operational amplifier to provide excellent response to load transients. The EUP7997 also incorporates a VSENSE pin to provide superior load regulation and a VREF output as a reference for chipset and DIMMs.

An additional feature found on the EUP7997 is an active low shutdown ($\overline{SD}$) pin. When $\overline{SD}$ is pulled low the VTT output will Tri-state providing a high impedance output, but, VREF will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

The EUP7997, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses.

FEATURES

- Input Voltage Range (AVIN): 3.15V to 5.5V
- VLDOIN Voltage Range : 1.5V to 3.3V
- Fast Transient Response Time
- Support DDR Ⅱ and DDRⅢ Requirements:
  Source/Sink 2A for DDR Ⅱ
  Source/Sink 2A for DDRⅢ
- Low-Current Shutdown Mode
- Over-Temperature Protection
- High Accuracy Output Voltage at Full-Load
- Low External Component Count
- Available in SOP-8 (EP) Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- DDR-Ⅱ and DDR-Ⅲ termination voltage

Typical Application Circuit

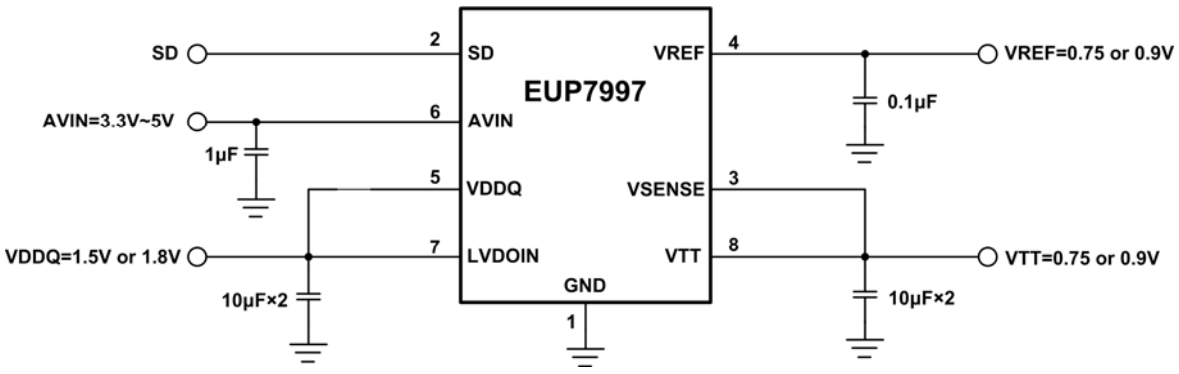

Figure 1. Recommended DDR-Ⅱ or DDR-Ⅲ Termination